REMARKS

This is intended as a full and complete response to the Office Action dated August 22, 2006, having a shortened statutory period for response set to expire on November 22, 2006. Please reconsider the claims pending in the application for reasons discussed below.

Claims 11-15, 17 and 20-27 are pending in the application. Claims 11-15, 17 and 20-27 remain pending following entry of this response.

Claim Rejections - 35 USC § 102

Claims 11-15, 17, 20-27 are rejected under 35 U.S.C. 102(e) as being anticipated by *Schoenfeld et al.* (Pub. U.S. 2005/0078539, hereinafter *Schoenfeld*). Applicant respectfully traverses this rejection.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

In this case, *Schoenfeld* does not disclose "each and every element as set forth in the claim". For example, with respect to Claim 11 and the claims that depend therefrom, *Schoenfeld* does not disclose monitoring, by a memory controller coupled with semiconductor memory devices, write operations to memory cells. The Examiner argues that *Schoenfeld* discloses monitoring, by a memory controller coupled with semiconductor memory devices, write operations to memory cells at Paragraphs 0005, 0027, and 0029 and in Claim 12 of *Schoenfeld*. However, the cited sections do not teach the claimed subject matter, as described below.

Schoenfeld is directed to a method for controlling a clock synchronizing circuit for a low power refresh operation. *See Schoenfeld*, Title. The method provided idles a

clock synchronizing circuit during a portion of time during execution of a refresh operation in a memory device. *See Schoenfeld*, Abstract. As described at Paragraph 0023, a delay-locked loop (DLL) control circuit can be used to put a DLL into an idle state during a memory cell refresh operation. *See Schoenfeld*, Paragraph 0023. The DLL control circuit 200 described with respect to Figure 2 in Paragraph 0023 can be substituted for DLL control circuit 125 depicted in Figure 1. *See Schoenfeld*, Figure 1; Paragraph 0023. As described in Paragraph 0027, by placing the DLL 123 into an idle state for at least a portion of an auto-refresh cycle, the average power consumed by the memory device during the auto-refresh operation can be reduced. *See Schoenfeld*, Paragraph 0027. As described in Paragraph 0029, the DLL cycles through entering the idle state and exiting the idle state for every auto-refresh operation. *See Schoenfeld*, Paragraph 0029. Claim 12 describes monitoring which is performed by a synchronizing clock circuit subsequent to re-enabling the synchronizing clock circuit. *See Schoenfeld*, Claim 12.

Thus, as described above, *Schoenfeld* is directed to idling a clock synchronizing circuit during a portion of time during execution of a refresh operation in a memory device. *See Schoenfeld*, Abstract. The sections of *Schoenfeld* cited by the Examiner fail to describe write operations. For this reason, the sections of *Schoenfeld* also fail to describe monitoring of a write operation by a memory controller. Accordingly, *Schoenfeld* does not describe monitoring, by a memory controller coupled with semiconductor memory devices, write operations to memory cells. Withdrawal of the rejection is respectfully requested.

With respect to Claim 11 and the claims that depend therefrom, *Schoenfeld* also does not disclose maintaining a plurality of bits indicative of rows containing memory cells involved in the monitored write operations on the memory controller. The Examiner states that *Schoenfeld* teaches the claimed subject matter at Paragraphs 0002 and 0026. Paragraph 0002 of *Schoenfeld* merely describes volatile memory and refreshing of memory cells generally. *See Schoenfeld*, Paragraph 0002. Paragraph 0026 of *Schoenfeld* describes using a DLL control circuit to generate a signal to place a DLL into an idle state. *See Schoenfeld,* Paragraph 0026. The paragraph describes initiating an auto-refresh operation and placing the DLL in an idle state as part of the

initiating operation. *See id.* The cited paragraph does not refer to a memory controller. *See id.* The cited section does not refer to a plurality of bits indicative of rows containing memory cells involved in a monitored write operation. *See id.* Accordingly, the sections of *Schoenfeld* cited by the Examiner do not describe maintaining a plurality of bits indicative of rows containing memory cells involved in the monitored write operations on the memory controller. Withdrawal of the rejection is respectfully requested.

With respect to Claim 13 and the claims that depend therefrom, *Schoenfeld* does not describe interface circuitry configured to receive a plurality of bits from a memory controller and to transfer the plurality of bits to the row state circuitry and refresh enable circuitry configured to limit the number of rows for which refresh requests are issued based on the bits of the row state circuitry. The sections of *Schoenfeld* cited by the Examiner merely refer to a refresh row address provided by a refresh counter when the memory device operates in an auto-refresh or self-refresh mode (Paragraph 0018) and a memory controller which applies bit data on a data bus (Paragraph 0022). The cited sections do not describe transferring a plurality of bits received from a memory controller to row state circuitry. The cited sections also do not describe refresh enable circuitry configured to limit the number of rows for which refresh requests are issued. Accordingly, *Schoenfeld* does not describe interface circuitry configured to receive a plurality of bits from a memory controller and to transfer the plurality of bits to the row state circuitry and refresh enable circuitry configured to limit the number of rows for which refresh requests are issued based on the bits of the row state circuitry. Withdrawal of the rejection is respectfully requested.

With respect to Claim 20 and the claims that depend therefrom, *Schoenfeld* does not describe a memory controller configured to monitor write operations to the memory device, generate the row data based on the monitored write operations, and transfer the row data to the memory device prior to placing the memory device in the self-refresh mode. For example, Paragraph 0022, cited by the Examiner, merely refers to a memory controller which applies bit data on a data bus. *See Schoenfeld,* Paragraph 0022. The Examiner also cites paragraphs 0026, 0027, and 0029 and Claim 12, which, as described above, do not refer to a memory controller or monitoring write operations

with a memory controller. Other sections cited by the Examiner (Paragraph 0008, Claim 6) also do not teach the claimed subject matter. Accordingly, *Schoenfeld* does not describe a memory controller configured to monitor write operations to the memory device, generate the row data based on the monitored write operations, and transfer the row data to the memory device prior to placing the memory device in the self-refresh mode. Withdrawal of the rejection is respectfully requested.

Conclusion

Having addressed all issues set out in the office action, Applicant respectfully submits that the claims are in condition for allowance and respectfully requests that the claims be allowed.

Respectfully submitted, and
S-signed pursuant to 37 CFR 1.4,

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